Japanese Kokai Patent Application No. Sho 62[1987]-249422

Translated from Japanese by the Ralph McElroy Translation Company
910 West Avenue, Austin, Texas 78701 USA

Code: 598-77469
Ref.: APPLIED DKT 306 D08

JAPANESE PATENT OFFICE
PATENT JOURNAL (A)
KOKAI PATENT APPLICATION NO. SHO 62[1987]-249422

Int. Cl.[4]:	H 01 L 21/302
Sequence Nos. for Office Use:	M-8223-5F
Filing No.:	Sho 61[1986]-92190
Filing Date:	April 23, 1986
Publication Date:	October 30, 1987
No. of Inventions:	1 (Total of 7 pages)
Examination Request:	Not filed

METHOD FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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[There are no amendments to this patent.]

Claims

1. Method for manufacturing semiconductor integrated circuit device characterized by the following facts: during etching to form grooves or holes on a substrate or during etching to form connecting holes on the substrate, a wall-surface deposit film made of a substance different from that of the substrate or the insulating film on the substrate is deposited and coated on the side wall of said grooves or holes on the substrate or the connecting holes on the substrate while said etching progresses; by controlling the deposition rate of said wall-surface deposit film and the etching rate, said grooves or holes or connecting holes are formed in a forward tapered shape.

2. Method for manufacturing semiconductor integrated circuit device described in Claim 1 characterized by the fact that said wall-surface deposit film is made of a substance released from the electrode material of the etching device or the electrode coating material for coating the portion of the electrode material exposed through the wafer.

3. Method for manufacturing semiconductor integrated circuit device described in Claim 1 characterized by the fact that the ratio of the deposition rate of said wall-surface deposit film to the etching rate of grooves or holes or connecting holes is 0.04 or larger, and the bias voltage applied on the electrode of the etching device has an absolute value of 350 V or larger.

4. Method for manufacturing semiconductor integrated circuit device described in Claim 1 characterized by the fact that said wall-surface deposit film is made of aluminum and oxygen or of aluminum.

Detailed explanation of the invention

Industrial application field

This invention pertains to an etching technology. In particular, this invention pertains to an etching technology for forming grooves or holes on a substrate or an etching technology for forming connecting holes on insulating film on a substrate.

Prior art

Dynamic RAM (DRAM) memory cells are made of selective MISFET [sic; MOSFET] and capacitive elements. In order to reduce the size, studies have focused on methods in which grooves or holes (referred to as grooves hereinafter) can be formed on a semiconductor substrate, and electrodes made of a dielectric film and a polysilicon film can be formed in the grooves to constitute the aforementioned capacitive elements. Said grooves are formed by reactive ion etching (RIE). RIE technology is described, for example, in the following reference: "Microdevices," Special issue of Nikkei Electronics, pp. 100-105, published by Nikkei McGraw Hill Co., August 22, 1983.

Problems to be solved by the invention

The present inventors studied the aforementioned technology and found the following problems.

When grooves are formed using RIE in the aforementioned technology, because the etching rate in the vertical direction is higher, the side walls of the grooves form vertically with respect to the upper surface of the substrate. In another possible case, etching takes place not only in the vertical direction, but also in the horizontal direction. Consequently, the grooves form in a barrel-like cross-sectional shape, that is, the middle portion of the groove bulges in comparison to the upper end of the groove. Consequently, when polysilicon film is embedded as electrodes in the grooves, cavities may form in the interior. This is a problem.

The purpose of this invention is to provide a technology which can form grooves or connecting holes on semiconductor substrates in a tapered shape (a shape inclined at an acute angle with respect to the principal surface of the substrate instead of vertical), so that the electroconductive film or insulating film can be well embedded in the aforementioned grooves or connecting holes.

Another purpose of this invention is to provide a technology which allows control of the taper angle (the angle between the incline surface and the principal surface of the substrate) of the aforementioned grooves or connecting holes during etching for forming grooves or connecting holes.

The purposes mentioned above and others of this invention will be clarified in the description and attached figures in this specification.

Means to solve the problems

The invention of this patent application can be summarized as follows.

During etching to form grooves or connecting holes, a wall-surface deposit film is deposited on the side walls of said grooves or connecting holes; by controlling the deposition

rate of the wall-surface deposit film and the etching rate of the semiconductor substrate or the etching rate of the insulating film for forming the connecting holes, it is possible to form said grooves or connecting holes in tapered a shape.

Function

By the aforementioned means, it is possible to embed an electroconductive film or insulating film in the grooves or connecting holes without the formation of cavities. Also, it is possible to control the taper angle of the grooves or connecting holes.

Application examples

In this application example, an example of this invention applying the technology for forming grooves on a substrate to form capacitive elements of DRAM memory cells is explained.

Figures 1-11 are diagrams illustrating the application example of this invention. Figure 1 is a schematic diagram illustrating the etching device, and Figures 2-11 are cross-sectional views of a memory cell in the DRAM manufacturing steps.

As shown in Figure 1, for cathode electrode (2) set in reaction container (1), its upper surface exposed next to wafer (3), that is, a substrate made of p-type single-crystal silicon carried on the cathode electrode is covered with electrode covering material (4) made of aluminum film or alumina (Al_2O_3) or the like. Electrode covering material (4) increases the efficiency of RIE.

(5) represents the reaction gas containing F, Cl, Br, etc. It is fed from the air inlet port (6A) of upper electrode (6) through upper electrode (6) into reaction container (1), and it is exhausted from exhaust port (8). Also, in Figure 1, for convenience, reaction gas (5) is indicated by arrows. In the area between cathode electrode (2) and upper electrode (6), plasma is formed by means of the RF power fed from RF (radio frequency) power source (7) to cathode electrode (2). (9) represents the ion sheath formed between cathode electrode (2) and the plasma. (10) represents a capacitor.

As shown in Figure 2, field insulating film (11) made of a silicon dioxide film and p-type channel stopper region (12) are formed on said substrate (3). Also, silicon dioxide film (13) is formed on the surface exposed through field insulating film (11) as an underlying film of etching mask (14) made of silicon dioxide film by means of, for example, CVD. For an etching mask (14) made of silicon dioxide film, the portion above groove (16) to be formed on substrate (3) later (see Figure 3) is selectively removed by etching using a mask made of a resist to form opening (15). The pattern of opening (15) defines the pattern of the opening on the upper end portion of groove (16).

After silicon dioxide film (13) exposed by said opening (15) is first removed, as shown in Figure 3(a), the surface of semiconductor substrate (3) exposed by opening (15) is etched to form groove (16). Said groove (16) is formed by means of ion assisted etching, with ions accelerated by plasma sheath (9) formed between cathode electrode (2) and the plasma to obtain kinetic energy and strike the surface of substrate (3) exposed by said opening (15). On the other hand, ions in said plasma also strike electrode covering material (4) to perform reverse sputtering for etching. Consequently, when electrode covering material (4) is made of aluminum, aluminum is released into the plasma, and, when electrode covering material (4) is made of alumina, aluminum and oxygen are released into the plasma. Said aluminum or aluminum and oxygen released into the plasma are redeposited on semiconductor substrate (3). This has been confirmed by the elemental analysis (AES) carried out by the present inventors. Said aluminum or aluminum and oxygen released into said plasma are deposited on the side surface of groove (16) to form wall-surface deposit film (17). As shown in Figures 3(a)-(d), wall-surface deposit film (17) grows in company with the progress of etching of semiconductor substrate (3). Consequently, the upper end portion of groove (16) becomes thicker. That is, the deeper the portion of groove (16), the narrower it is. In Figures 3(a)-(d), groove (16) is illustrated as narrowing stepwise. However, this is just for facilitating illustration. In practice, narrowing takes place continuously as shown in Figure 4.

Figure 4 is a diagram illustrating the shape of groove (16) when groove (16) reaches the end point with a prescribed depth. As shown in Figure 4, width L_A of the bottom portion of groove (16) is determined by width L_B of the narrowest portion due to wall-surface deposit film (17) grown on the two side surfaces of groove (16).

In this way, according to the technology for forming groove (16) in this application example, the cross section of groove (16) is a forward tapered shape, that is, the deeper the portion of groove (16), the narrower it is.

In the following, the method for controlling the taper angle of groove (16) will be explained with reference to Figures 12 and 13.

Figure 12 is a cross-sectional view of groove (16) for illustrating the taper angle in the case when the deposition rate (D.R) of wall-surface deposit film (17) and the etching rate (E.R) of semiconductor substrate (3) are changed. Figure 13 includes a graph illustrating the dependence of the ratio of the deposition rate of wall-surface deposit film (17) to the etching rate of semiconductor substrate (3) on self-bias voltage Vdc (Figure 13(a)), and a graph illustrating the dependence of taper angle θ on the ratio of the deposition rate of wall-surface deposit film (17) to the etching rate of semiconductor substrate (3) (Figure 13(b)).

In this application example, taper angle θ of groove (16) refers to the angle formed between the line parallel to the inner surface of semiconductor substrate (3) and the side surface of groove (16), in particular, the side surface of the bottom portion of groove (16).

Figure 12(a) is a diagram illustrating the case when groove (16) is formed at a low rate of deposition of wall-surface deposit film (17). In this case, taper angle θ increases. Figure 12(b) is a diagram illustrating the case when the deposition rate of wall-surface deposit film (17) is lower. In this case, taper angle θ decreases. Figure 12(c) is a diagram illustrating the case when the etching rate of semiconductor substrate (3) is higher. In this case, taper angle θ increases. Figure 12(d) is a diagram illustrating the case when the etching rate of semiconductor substrate (3) is lower. In this case, taper angle θ decreases.

Supposing the diameter of the bottom portion of groove (16) is d, the diameter of opening (15) on etching mask (14) is D, and the thickness of wall-surface deposit film (17) is t, one has d=D-2t. That is, measurement d depends on the thickness of wall-surface deposit film (17).

According to experiments performed by the present inventors, as shown in Figure 13(b), in order to have a forward tapered shape with a taper angle θ smaller than 90°, the ratio of the deposition rate of wall-surface deposit film (17) to the etching rate of semiconductor substrate (3), that is, deposition rate of wall-surface deposit film (17)/etching rate of semiconductor substrate (3), should be 0.04 or larger. Also, in order for the ratio of the deposition rate of wall-surface deposit film (17) to the etching rate of semiconductor substrate (3) to be 0.04 or larger, the absolute value of the self-bias Vdc of plasma sheath (9) (Figure 1) should be 350 V or higher. When groove (16) is formed under these conditions, it is possible to form groove (16) with a vertical upper half and a forward tapered lower half. Also, as shown in Figure 4, as ions (18) for etching strike wall-surface deposit film (17), the portion above the most protruding portion as the boundary tends to become thinner.

After groove (16) has formed, as shown in Figure 5, wall-surface deposit film (17) is removed with an acid solution. The opening diameter of the upper end portion of groove (16) is defined by the opening on the etching mask (14). The size of opening (15) is the same as that before the start of etching of semiconductor substrate (3), that is, the size when opening (15) is formed on etching mask (14). This is because the etching ions on etching mask (14) in opening portion (15) are prevented from striking by wall-surface deposit film (17) in this case. Consequently, there is no change in the measurements of mask (14) and groove (16).

After the end of etching, etching mask (14) and underlying film (13) made of a silicon dioxide film are removed.

Then, as shown in Figure 6, the entire exposed surface of semiconductor substrate (3) is thermally oxidized, so as to form dielectric film (19) made of silicon dioxide film. Also, dielectric film (19) may have a 3-layer film structure prepared by forming a silicon nitride film

by CVD on a silicon dioxide film by thermal oxidation, followed by oxidizing the silicon nitride film to form a silicon dioxide film.

Then, as shown in Figure 7, for example, CVD is used to form polysilicon film (20) on the entire surface of semiconductor substrate (3). As groove (16) is formed in a forward tapered shape, polysilicon film (20) does not overhang in the upper end portion of groove (16). Also, no gaps are formed between polysilicon film (20) and the wall surface of groove (16). As said polysilicon film (20) continues to grow, as shown in Figure 8, it is completely embedded in groove (16). Then, as shown in Figure 9, polysilicon film (20) is etched (etchback) from its upper surface by RIE, so that dielectric film (19) on the upper surface of semiconductor substrate (3) is exposed. That is, polysilicon film (20) is left only inside groove (16). In this way, as groove (16) is formed in the forward tapered shape, no cavities form inside groove (16). Also, during etchback, there is no opening in the upper end portion of groove (16).

Then, as shown in Figure 10, for example, by means of CVD, polysilicon film (20) is formed on semiconductor substrate (3), and, by means of etching using a resist mask, said polysilicon film (20) is patterned to form electroconductive plate (20). Said resist mask is removed after etching. Also, electroconductive plate (20) is composed of polysilicon film (20) in groove (16) and polysilicon film (20) on semiconductor substrate (3). Then, dielectric film (19) exposed through electroconductive plate (20) is etched off. Then, electroconductive plate (20) is oxidized to form insulating film (21) made of a silicon dioxide film. When insulating film (21) is formed, after removal of the silicon dioxide film formed on the surface of semiconductor substrate (3) exposed by insulating film (21) and field insulating film (11), the surface of semiconductor substrate (3) is oxidized, so that gate insulating film (22) made of a silicon dioxide film is formed.

Then, as shown in Figure 11, on the polysilicon film, the following parts are formed: gate electrodes (23) and word lines WL with the so-called polycide structure formed by laminating Mo, W, Ta, Ti, or other high-melting point metal films or their silicide films; side wall spacers (24) made of silicon dioxide film; n-type semiconductor regions (25) and n^+-type semiconductor regions (26) that form the source and drain regions; insulating film (27) made of, for example, phosphorus silicate glass (PSG) film; connecting holes (28); and data lines DL made of an aluminum film. After this, the operation in this application example ends.

Also, when connecting hole (28) is formed, the operation may be performed in the same way as in the method for forming said groove (16). That is, wall-surface deposit film (17) made of aluminum or aluminum and oxygen is deposited on the wall surface of connecting hole (28), while etching is carried out, so that connecting hole (28) is formed in a forward tapered shape.

The aforementioned application example has the following effects.

(1) Wall-surface deposit film (17) is formed on the side surface of groove (16). By controlling the ratio of the deposition rate of said wall-surface deposit film (17) to the etching rate of semiconductor substrate (3), or by controlling the self-bias potential, said groove (16) is formed. In this way, the deep portion of groove (16), in particular, the portion deeper than the middle portion, has the smaller diameter of groove (16). Consequently, groove (16) is formed in a forward tapered shape.

(2) While wall-surface deposit film (17) is deposited on the side surface of groove (16), etching of semiconductor substrate (3) is carried out. In this way, because the opening portion on the upper end portion of groove (16) is not struck by the etching ions, it is possible to form said groove (16) without a change in the measurement between groove (16) and etching mask (14).

(3) In said step (1), the polysilicon film for forming electroconductive plate (20) is embedded well in groove (16). Consequently, it is possible to improve the flatness of electroconductive plate (20).

(4) In said step (3), it is possible to improve the insulating voltage rating between word line WL extending on electroconductive plate (20) and electroconductive plate (20).

(5) By forming connecting hole (28) in the forward tapered shape, there is no wire breakage of data DL in connecting hole (28), so that it is possible to improve the reliability of the semiconductor integrated circuit device.

In the above, this invention has been explained in detail with reference to an application example. However, this invention is not limited to the aforementioned application example. Various changes may be made as long as the gist is observed.

For example, electrode covering material (4) is not limited to aluminum and alumina. Other materials, such as silicon carbide, carbon, hydrocarbons (plastics), etc., may also be used. As long as sputtering can be performed by the etching gas of RIE, any of these materials may be used.

Also, this invention may be adopted in the technology in which groove (16) is formed between semiconductor elements, and, after oxidation of the inner wall of groove (16) to form a silicon dioxide film, a polysilicon film is embedded in groove (16) so as to electrically isolate said semiconductor elements.

Effects of the invention

The following are the typical effects that can be realized by the invention disclosed in this patent application.

It is possible to form grooves in a forward tapered shape on a semiconductor substrate. Consequently, it is possible to embed the interior of the grooves better by means of an electroconductive film or insulating film.

Also, it is possible to control the taper angle of said grooves during the etching step.

Brief description of the figures

Figure 1 is a schematic diagram illustrating the RIE device.

Figures 2, 3(a)-(d) through Figure 11 are cross-sectional views of the memory cell in the various DRAM manufacturing steps.

Figures 12(a)-(d) are cross-sectional views of the groove illustrating the RIE etching characteristics of the semiconductor substrate.

Figures 13(a) and (b) are graphs illustrating the RIE etching characteristics of the semiconductor substrate.

1	Reaction container
2	Cathode electrode
3	Semiconductor substrate (wafer)
4	Electrode covering material (aluminum or alumina)
5	Etching gas
6	Upper electrode
6A	Gas inlet port
7	RF power source
8	Gas exhaust port
9	Ion sheath
10	Capacitor
11	Field insulating film
12	Channel stopper
13	Underlying film (SiO_2)
14	Etching mask (SiO_2)
15	Opening
16	Groove
17	Wall-surface deposit film (aluminum or aluminum and oxygen)
17A	Tapering portion of wall-surface deposit film
18	Ion
19	Dielectric film
20	Electroconductive plate
21, 27	Insulating film
22	Gate insulating film
23	Gate electrode

24 Side wall spacer
WL Word line
DL Data line
25, 26 Semiconductor region
28 Connecting hole

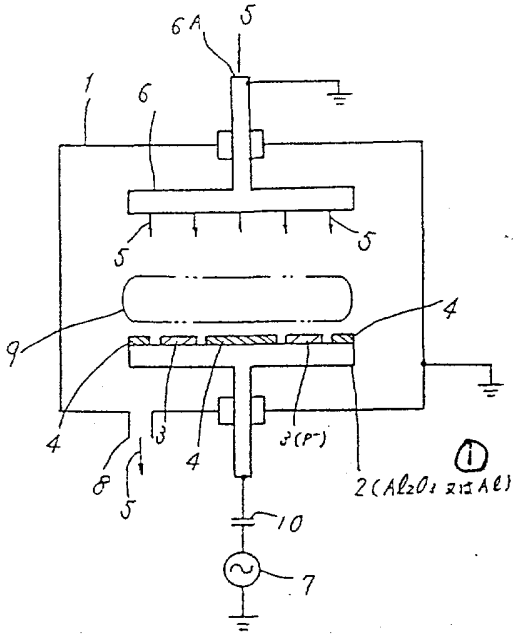

Figure 1

Key: 1 (Al_2O_3 or Al)

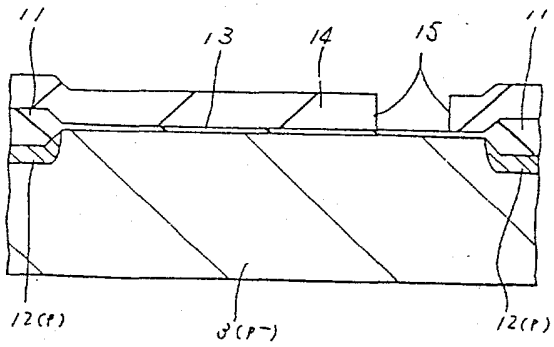

Figure 2

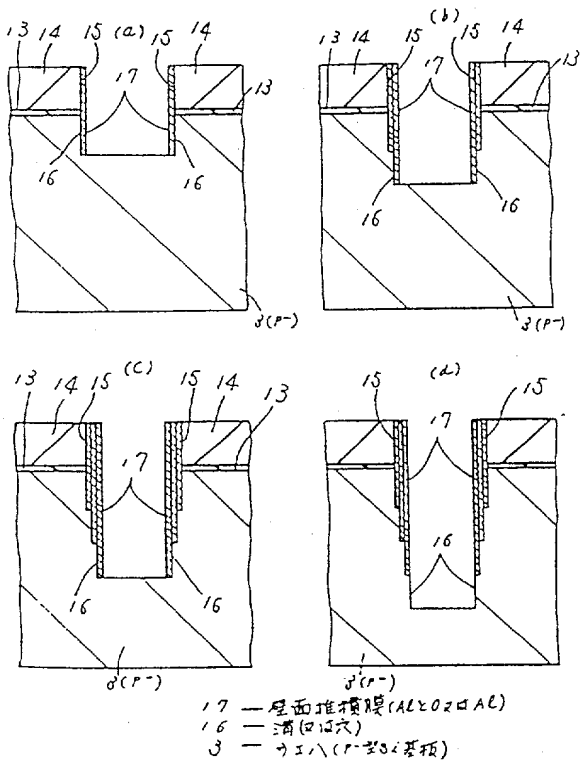

Figure 3

Key: 17 Wall-surface deposit film (Al and O_2 or Al)
16 Groove (or hole)
3 Wafer (p^--type Si substrate)

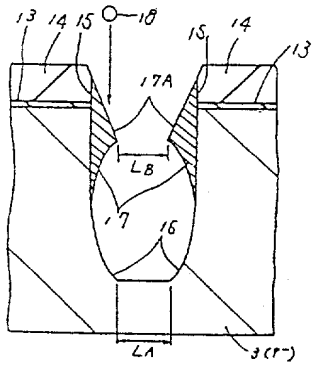

Figure 4

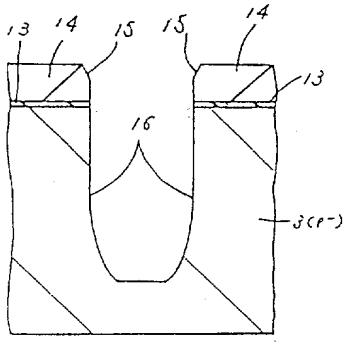

Figure 5

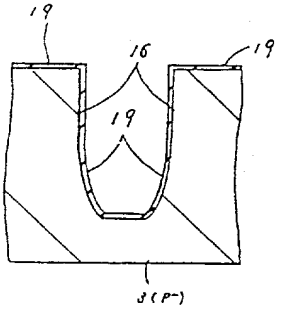

Figure 6

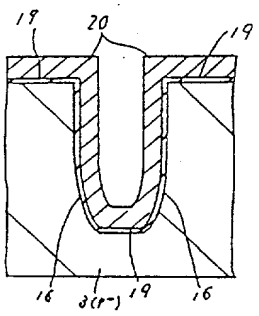

Figure 7

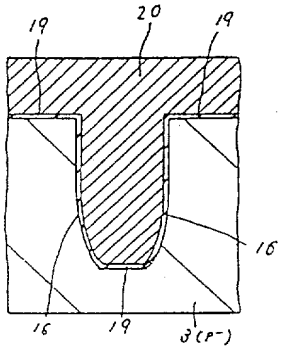

Figure 8

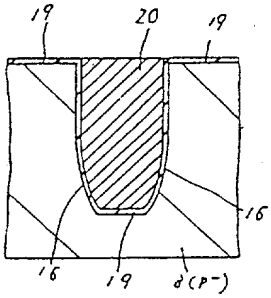

Figure 9

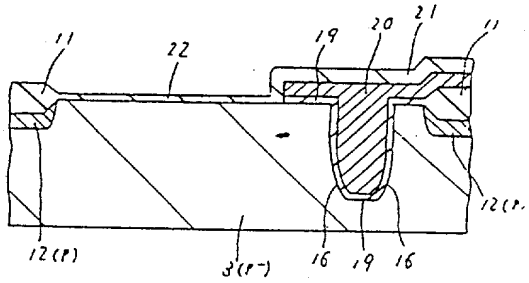

Figure 10

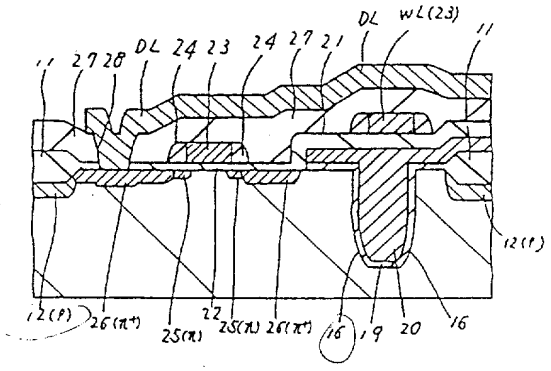

Figure 11

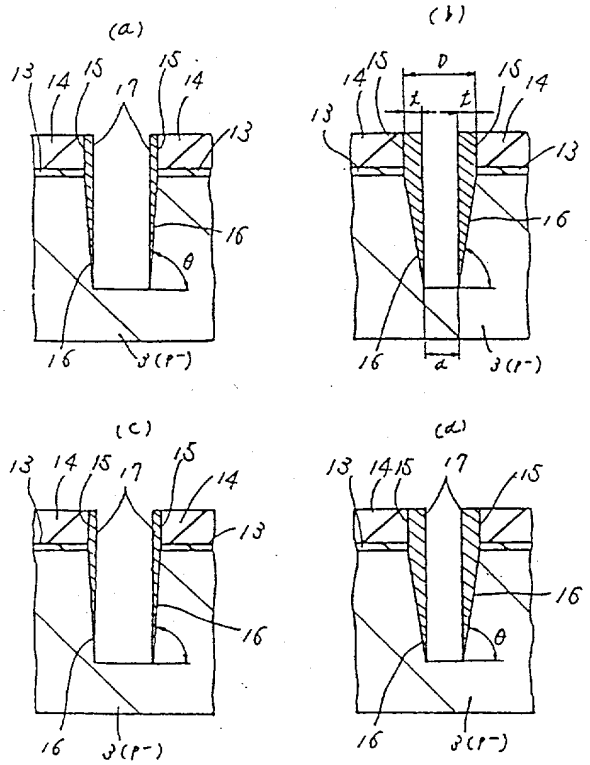

Figure 12

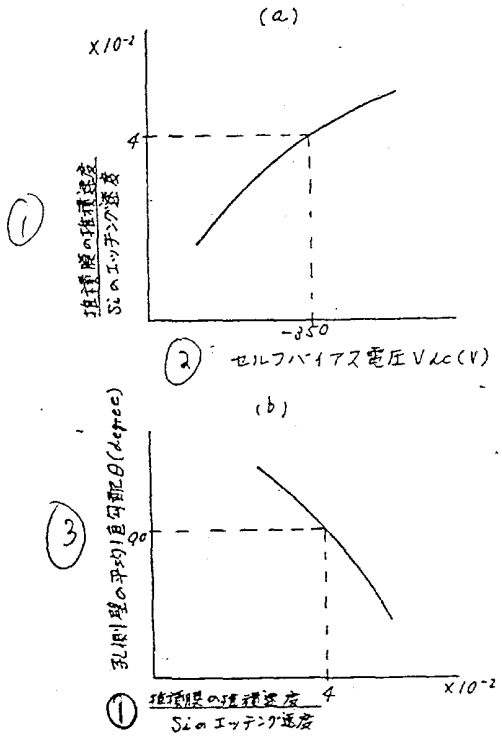

Figure 13

Key: 1 Deposition rate of deposited film/etching rate of Si
2 Self-bias voltage vdc (v)
3 Average gradient of side wall of hole θ (degrees)